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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/551,837	10/03/2005	Soha M. N. Hassoun	TUFTS-002AUS	4243
22494 7590 11/13/2007 DALY, CROWLEY, MOFFORD & DURKEE, LLP SUITE 301A 354A TURNPIKE STREET CANTON, MA 02021-2714			EXAMINER TAT, BINH C	
			ART UNIT 2825	PAPER NUMBER
			MAIL DATE 11/13/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/551,837

Applicant(s)

HASSOUN ET AL.

Examiner

Binh C. Tat

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 10/25/07.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) 1-12 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 13-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 October 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 01/27/06.
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- ☐ Notice of Informal Patent Application
- ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

1. This office action is in response to restriction election file on 10/25/07. The examiner acknowledges: the election of group II, claims 13-22 without traverse. The cancellation of non-election claims 1-12.

#### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3-6 re rejected under 35 U.S.C. 102(e) as being anticipated by Ashar et al. (US Pub. 6745160).

3. As to claim 13, Ashar et al. teach a method of scheduling processing in a hardware threaded circuit, comprising: receiving inputs corresponding to unthreaded processing of an application (see fig 15 col 4 line 8 to col 6 line 11); receiving information including processing element resources, a number of processing elements, and a window size corresponding to a number of downstream processing states to be examined (see fig 15 col 26 line 16 to col 29 line 11); and generating a hardware threaded schedule for processing the application with at least first and second one of the processing elements being interconnected to enable dynamic resource sharing (see fig 10-15 col 26 line 30 to col 30 line 48, and summary).

4. As to claim 14, Ashar et al. teach further including synthesizing the hardware threaded schedule to an Application Specific Circuit (ASC) (see col 3 line 60 to col 7 line 40).
5. As to claim 15, Ashar et al. teach further including synthesizing the hardware schedule to maximize throughput (see col 1 line 8 to col 4 line 68).
6. As to claim 16, Ashar et al. teach further including synthesizing the hardware threaded schedule to reduce power consumption (see col 6 line 32 to col 7 line 39).
7. As to claim 17, Ashar et al. teach further including receiving resource constraint information for the processing elements (see fig 10-15 col 26 line 30 to col 30 line 48, and summary).
8. As to claim 18, Ashar et al. teach a hardware threaded circuit system, comprising: a memory (see fig 15 col 12 line 43 to col 13 line 33); a task manager coupled to the memory (see fig 15 col 12 line 43 to col 13 line 33); and a plurality of processing elements coupled to the task manager, wherein first and second ones of the plurality of processing elements are interconnected for hardware threaded processing to enable dynamic borrowing of processing resources associated with the second one of the plurality of processing elements by the first one of the plurality of processing elements (see fig 10-15, col 12 line 24 to col 16 line 68, and col 26 line 30 to col 30 line 48).
9. As to claim 19, Ashar et al. teach wherein the circuit maximizes throughput (see col 1 line 8 to col 4 line 68).
10. As to claim 20, Ashar et al. teach wherein the circuit reduces power consumption compared to a non-threaded processing for substantially similar system wait times (see col 6 line 32 to col 7 line 39).

*11.* As to claim 21, Ashar et al. teach wherein the first and second processing elements each include a first type of resource and a second type of resource and a multiplexer such that the interconnection includes at least one input signal being provided to the first type of resource in the first and second processing elements (see fig 10-15 col 26 line 30 to col 30 line 48, and summary).

*12.* As to claim 22, Ashar et al. teach wherein the interconnection includes a connection from an output of the second processing element first type of resource to the first processing element (see fig 10-15 col 26 line 30 to col 30 line 48, and summary).

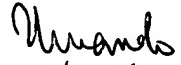
***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is 571 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Binh Tat  
Art unit 2825  
November 07, 2007

  
11/08/2007  
**THUAN V. DO**  
**PRIMARY PATENT EXAMINER**